

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHUICHI EUNO, YOSHINORI OKUMURA,
SHIGENOBU MAEDA, and SHIGETO MAEGAWA

Appeal No. 2003-2107
Application No. 09/429,283

HEARD: April 13, 2004

Before GROSS, BARRY, and SAADAT, *Administrative Patent Judges*.
GROSS, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 14 through 27, which are all of the claims pending in this application.

Appellants' invention relates to a method of manufacturing a semiconductor device having two types of transistors formed on a single substrate. The method includes introducing an impurity into the polysilicon layer of both transistors, wherein the impurity dosage for one transistor differs from the impurity dosage for the other. Claim 14 is illustrative of the claimed invention, and it reads as follows:

14. A method of manufacturing a semiconductor device in which there are first and second types of transistors formed on a single semiconductor substrate, comprising the steps of:

(a) selectively forming a field oxide film on a main surface of said semiconductor substrate to thereby define first and second regions in which said first and said second types of transistors are formed;

(b) forming an oxide film on said first and said second active regions; and

(c) forming a control electrode of a polysilicon layer on said first and said second regions,

wherein said step (c) includes the steps of:

(c-1) introducing an impurity of the same conductivity as a source/drain layer into said polysilicon layer within said first active region at a relatively low dose n1; and

(c-2) introducing said impurity into said polysilicon layer within said second active region at a relatively high dose n2 while introducing nitrogen into a lower portion of said polysilicon layer within said second active region at a dose n3.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Choi	5,780,330	Jul. 14, 1998 (filed Jun. 28, 1996)
Gardner et al. (Garner)	6,004,849	Dec. 21, 1999 (filed Aug. 15, 1997)
Chishima (Japanese Kokai Patent)	JP 4-157766	May 29, 1992

A. I. Chou et al. (Chou), "The Effects of Nitrogen Implant into Gate Electrode on the Characteristics of Dual-Gate MOSFETs with Ultra-thin Oxide and Oxynitrides," IEEE 174-77 (August 4, 1977)

S.M. Sze (Sze), VLSI Technology 493-94 (2d ed., McGraw-Hill 1988)

Takashi Kuroi et al. (Kuroi), "The Impact of Nitrogen Implantation into Highly Doped Polysilicon Gates for Highly Reliable and High-Performance Sub-Quarter-Micron Dual-Gate Complementary Metal Oxide Semiconductor," 34 Japanese Journal of Appl. Phys., Pt. 1, No. 2B, 771-75 (February 1995)

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Claims 14 through 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chishima in view of Gardner, Choi, Chou, Kuroi, and Sze.

Reference is made to the Examiner's Answer (Paper No. 21, mailed October 2, 2002) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 18, filed May 20, 2002) and Reply Brief (Paper No. 22, filed December 2, 2002) for the appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 14 through 27.

Independent claim 14 recites introducing an impurity into each of the two transistors, but with different dosages. In independent claim 16, the control electrode for each of the two transistors includes nitrogen, and then extra nitrogen is added to the control electrode of only one of the transistors.

Independent claim 19 recites nitrogen of a first concentration for the control electrode of one transistor and nitrogen of a second concentration different from the first concentration for the control electrode of the second transistor. All of the claims thus require that at least some impurity (nitrogen for

claims 16 and 19) is introduced into both transistors and that the amount for one is different from the amount for the other.

The examiner relies upon Chishima, Gardner, Choi, Chou, Kuroi, and Sze in rejecting all of the claims. Specifically, the examiner states (Answer, pages 3-5) that Chishima discloses nitrogen in the p-channel transistor but not in the n-channel transistor, Choi discloses implanting nitrogen in p-type transistors, and Gardner discloses that the threshold voltage depends on the concentration of dopants in the gate of a MOSFET and "the formation of MOSFETs having different concentrations of dopant on the same wafer thus establishing dopant concentration in the gate of a MOSFET to be a result effective variable." The examiner further states that Chou discloses "the effects of different concentrations of nitrogen in the gate of a MOSFET with respect to B, which is a p-type dopant and As, which is an n-type dopant, thus establishing nitrogen concentration in the gate of a MOSFET to be a result effective variable for both p-type and n-type gates," and Kuroi discloses "the effects of different nitrogen concentrations and dopant concentrations in the gate of a MOSFET for both p-type and n-type gates thus establishing concentrations of dopant and nitrogen together to be a result effective variable." Although the examiner includes Sze in the statement of the rejection, we find no explanation as to why the examiner included Sze.

Rather than try to decipher the examiner's reasoning for combining the references, we will analyze each reference for its teachings and combinability with the other references applied by the examiner. We begin with Chishima.

As indicated by the examiner (Answer, page 5), Chishima teaches implanting nitrogen in the p-channel area. However, Chishima also explains (translation, page 4) that for an n-channel MOSFET, nitrogen doping "leads to an undesired increase in the gate capacitance. Consequently, **doping of nitrogen N in the n-channel MOSFET region should be avoided**" (emphasis ours).

We note that claim 14 encompasses impurities other than nitrogen; however, nitrogen is the only impurity discussed by Chishima with regard to both transistors. Accordingly, Chishima teaches away from the claimed invention. Further, the Federal Circuit has held that "a proposed modification [is] inappropriate for an obviousness inquiry when the modification render[s] the prior art reference inoperable for its intended purpose." *In re Fritch*, 972 F.2d 1260, 1265-66, n.12, 23 USPQ2d 1780, 1783, n.12, citing *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Thus, it would not have been obvious to modify Chishima to include doping the n-channel MOSFET.

Choi discloses two different transistors on the same chip and, as recognized by the examiner (Answer, page 5), discusses nitrogen implantation for the p-type MOSFET (to reduce the penetration of boron through the gate oxide layer). However, Choi teaches (column 2, lines 2-3) that "nitrogen incorporation degrades p-channel mobility which is also undesirable." Nonetheless, Choi discloses (column 8, lines 16-18) an embodiment which includes nitrogen implantation, but with no suggestion to implant nitrogen in the n-type MOSFET with a different concentration than that used for the p-type MOSFET. Further, as with Chishima, no impurity other than nitrogen is discussed with respect to both transistors.

Gardner (column 10, lines 21-26) states generally that the amount of dopant in the gate affects the threshold voltage. However, Gardner does not specify how the amount of dopant affects the threshold voltage, and particularly how nitrogen affects it. Therefore, though the amount of dopant might be a result effective variable, as asserted by the examiner, Gardner's teachings are insufficient to reach that conclusion.

The examiner's synopsis of Chou is partially correct. That is, Chou teaches nitrogen implantation for PMOSFETs and shows how different dosages of nitrogen affect flatband voltage shift, oxide reliability, sheet resistance, and poly depletion effects

in PMOSFETs. However, Chou does not teach nitrogen implantation for n-type MOSFETs. Instead, Chou states (second column on page 176) that "N+ poly NMOSFET gm and threshold voltage are not affected by nitrogen implant." Accordingly, although Chou suggests that nitrogen concentration is a result effective variable for PMOSFETs, Chou fails to suggest implanting nitrogen in NMOSFETs at a concentration different from that used for the PMOSFETs. Further, Chou does not disclose implanting any other impurities in both transistors.

Kuroi shows (in Figure 1) a PMOSFET and an NMOSFET, each with nitrogen implanted gates. As recognized by the examiner (Answer, page 5), Kuroi graphs the effects of different nitrogen concentrations for PMOSFETs and NMOSFETs. However, Kuroi (on page 772) implants the nitrogen ions into the polysilicon film for both MOSFETs at the same time, thereby suggesting the same high amounts of nitrogen for both the PMOSFET and the NMOSFET. Accordingly, Kuroi does not teach or suggest that the amounts of nitrogen should be different for the two MOSFETs. Further, Kuroi does not disclose any other impurities for both transistors.

As indicated *supra*, the examiner includes no explanation as to the relevance of Sze. Further, we find nothing in Sze regarding concentrations of nitrogen (or other impurities) in PMOSFETs and NMOSFETs. Therefore, none of the references teaches

or suggests implanting nitrogen (or another impurity) in both a PMOSFET and also an NMOSFET, but with different concentrations. Consequently, the examiner has failed to establish a ***prima facie*** case of obviousness, and we cannot sustain the rejection of claims 14 through 27.

The decision of the examiner rejecting claims 14 through 27 under 35 U.S.C. § 103 is reversed.

Anita Pelman Gross

LANCE LEONARD BARRY
Administrative Patent Judge

Mahshid D. Dadgar

APG:clm

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